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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/654,893	09/05/2003	Kiyoshi Hayase	242358US2	6644

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EXAMINER	
SCHELL, JOSEPH O	

ART UNIT	PAPER NUMBER
2114	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/654,893	HAYASE, KIYOSHI	
	Examiner	Art Unit	
	Joseph Schell	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claims 1-10 have been examined.

Claims 1-10 have been rejected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-3 and 6 are rejected under 35 U.S.C. 103(a) as being obvious over Debling (US Patent 6,973,592).

2. As per claim 1, Debling ('592) discloses a multiprocessor system comprising:

a plurality of processors (column 3 lines 59-63);

at least one debug executing unit for executing the debugging of said plurality of processors (column 3 lines 59-63, the on-chip emulator);

at least one controller for controlling said debug executing unit (column 3 lines 63-65, the USB interface controller);

a terminal to be connected to an external debugging device (column 4 lines 3-4); and

a selecting circuit for selecting, from among said plurality of processors, part or all of said plurality of processor to be debugged (column 3 lines 63 through column 4 line 2, the USB hub).

Although in the previous embodiment (as depicted by figure 1) both USB and JTAG ports are included for debugging, Debling ('592) does not explicitly disclose the multiprocessor system including a set of terminals for connecting to an external debugging device. Within the second embodiment, Debling ('592) states that JTAG circuitry as shown in the first figure may also be provided but it has been omitted for clarity (column 4 lines 1-2).

At the time of invention it would have been obvious to a person of ordinary skill in the art to include additional circuitry and ports for JTAG debugging of the processors. This would have been obvious because a JTAG port would allow the daisy-chaining of other devices for simultaneous debugging (column 4 lines 29-33).

3. As per claim 2, Debling ('592) teaches the multiprocessor system according to claim 1, wherein

said plurality of processors comprise first and second processors (as shown in figure 2, elements 110),

said debug executing unit comprises a first debug executing unit connected to said first processor and a second debug executing unit connected to said second processor (as shown in figure 2, each processor (110) has an on-chip emulator (120)),

said controller comprises a first controller connected to said first debug executing unit and a second controller connected to second debug executing unit (as shown in figure 2, each emulator (120) has a USB interface controller (140)), and

said selecting circuit inputs, to one or both of said first and second controllers, a debugging signal that is provided from said debugging device through said set of terminals (column 4 lines 3-4 and figure 2, the USB hub performs signal routing).

4. As per claim 3, Debling ('592) discloses the multiprocessor system according to claim 1, wherein

said plurality of processors comprise first and second processors (as shown in figure 2, elements 110),

said debug executing unit comprises a first debug executing unit connected to said first processor and a second debug executing unit connected to said second processor (as shown in figure 2, each processor (110) has an on-chip emulator (120)),

said selecting circuit is connected between said first and second debug executing units and said controller (column 4 lines 5-9, the controller is the host system. As shown in figure 2, the selecting circuit is between the outside host connected by USB and each on-chip emulator),

said controller is connected to said set of terminals (column 4 lines 5-9), and

said selecting circuit inputs, to one or both of said first and second debug executing units, a debugging signal outputted from said controller (column 4 lines 5-9, programs are downloaded from the host system for performing debugging).

5. As per claim 6, Debling ('592) discloses the multiprocessor system according to claim 1, wherein said selecting circuit selects said part or all of said plurality of processors to be debugged, on the basis of a select signal inputted to a given terminal from the outside (column 5 lines 42-48).

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Debling ('592) in view of Miura (US Patent 6,918,058).

Debling ('592) discloses the multiprocessor system according to claim 1, wherein

said plurality of processors comprise first and second processors (as shown in figure 2, elements 110),

said selecting circuit is connected between said first and second processor and said debug executing unit (as shown in figure 2, the USB hub (170) is between processors), and

said debug executing unit is connected to said set of terminals (as argued for claim 1, the inclusion of a JTAG port for each processor would have been obvious).

Debling ('592) does not explicitly disclose the system wherein said selecting circuit

inputs, to one or both of said first and second processors, a debugging signal outputted from said debug executing unit. In the multiprocessor system disclosed by Debling ('592), each processor has its own on-chip emulator (as shown by figure 2).

Miura ('058) teaches a system that uses a single debugging module to allow an external debugging tool to debug two processors (as shown by figure **1** with the Debugging Tool (3) connected to the single Debugging Module (13) which is connected to first and second microprocessors (elements 10 and 12)).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the debugging system disclosed by Debling ('592) wherein each processor has an associated on-chip emulator, such that a single debugging unit is used for all the processors. This modification would have been obvious because it would avoid unnecessary enlargement of the system and the increased manufacturing costs thereof.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Debling ('592) in view of Windows 2000 Device Driver Book.

Debling ('592) discloses the multiprocessor system according to claim 1. Debling ('592) does not explicitly disclose the system wherein said selecting circuit selects said part or all of said plurality of processors to be debugged on the basis of setting of a given register.

Windows 2000 Device Driver Book teaches general information about using device registers for peripheral control.

At the time of invention it would have been obvious to a person of ordinary skill in the art to implement register control within the system disclosed by Debling ('592). This modification would have been obvious because device drivers communicate with a peripheral by reading and writing registers associated with the device (Windows 2000 Device Driver Book chapter 2, section on Device Registers).

8. Claims 7-8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Debling ('592) in view of Mantey (US Patent Application Publication 2003/0023793).

9. As per claim 7, Debling ('592) discloses a multiprocessor system comprising:

first and second processors (as shown in figure 2, elements 110);

a first debug executing unit connected to said first processor and a second debug executing unit connected to said second processor (as shown in figure 2, each processor (110) has an on-chip emulator (120));

a first controller connected to said first debug executing unit and a second controller connected to said second debug executing unit (as shown in figure 2, each emulator (120) has a USB interface controller (140));

a selecting circuit connected between said first set of terminals and said first and second controllers (element 170 of figure 2, the USB hub);

and wherein in a second mode in which said debugging device is connected only to said first set of terminals, said selecting circuit inputs, to on or both of said first and second controllers, a debugging signal provided from said debugging device through said first set of terminals (column 4 lines 5-9, programs are conveyed from the host system through the USB hut to an on-chip emulator).

Although in the previous embodiment (as depicted by figure 1) both USB and JTAG ports are included for debugging, Debling ('592) does not explicitly disclose the multiprocessor system including a set of terminals for connecting to an external debugging device. Within the second embodiment, Debling ('592) states that JTAG circuitry as shown in the first figure may also be provided but it has been omitted for clarity (column 4 lines 1-2).

At the time of invention it would have been obvious to a person of ordinary skill in the art to include additional circuitry and ports for JTAG debugging of the processors. This would have been obvious because a JTAG port would allow the daisy-chaining of other devices for simultaneous debugging (column 4 lines 29-33).

Debling ('592) additionally does not disclose the system wherein, in a first mode in which debugging devices are connected respectively to said first and second sets of

terminals, said selecting circuit connects said first controller and said first set of terminals, and connects said second controller and said second set of terminals.

Mantey ('793) teaches a system that performs JTAG debugging of multiple processing devices (in this case FPGAs) on separate boards (see abstract). As shown by Figure 2, the system employs a central board (element 216) with separate JTAG ports for each board.

At the time of invention it would have additionally been obvious to a person of ordinary skill in the art to include a separate JTAG port connected to the external debug controller for each processor, thereby allowing each controller to communicate over a separate port. This modification would have been obvious because when multiple devices are connected to a JTAG chain it slows access for the debugger (Mantey ('793) paragraph 18).

10. As per claim 8, Debling ('592) in view of Mantey ('793) discloses the multiprocessor system according to claim 7, wherein said first mode and said second mode are switched on the basis of a select signal inputted to a given terminal from outside (Debling ('592) column 5 lines 42-48).

11. As per claim 10, Debling ('592) in view of Mantey ('793) discloses the multiprocessor system according to claim 7, further comprising a detecting circuit for

detecting whether said debugging device is connected to said second set of terminals (Debling ('592) column 4 lines 63-64, the plug-and-play feature of USB means it automatically detects when a device is plugged into a USB port).

Neither Debling ('592) nor Mantey ('793) explicitly discloses the system wherein said first mode and said second mode are switched on the basis of a result detected by said detecting circuit. However, as USB devices are plug-and-play, it would be obvious that when a device is plugged into the USB debugger that debugging information would be expected over the USB port connected to each debugger (as shown by Debling ('592) figure 2) instead of over a JTAG port.

12. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Debling ('592) in view Mantey ('793) as applied to claim 7, and in further view of Windows 2000 Device Driver Book.

Debling ('592) in view of Mantey ('793) discloses the multiprocessor system according to claim 7. Debling ('592) in view of Mantey ('793) does not explicitly disclose the system wherein said selecting circuit selects said part or all of said plurality of processors to be debugged on the basis of setting of a given register.

Windows 2000 Device Driver Book teaches general information about using device registers for peripheral control.

At the time of invention it would have been obvious to a person of ordinary skill in the art to implement register control within the system disclosed by Debling ('592). This modification would have been obvious because device drivers communicate with a peripheral by reading and writing registers associated with the device (Windows 2000 Device Driver Book chapter 2, section on Device Registers).

Conclusion

The prior art made of record on accompanying PTO 892 form and not relied upon is considered pertinent to applicant's disclosure. Specifically, Jahnke ('722) teaches a multiprocessor system with separate TAP controllers for each processor and a multiplexer for directing external debugging commands.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Schell whose telephone number is (571) 272-8186. The examiner can normally be reached on Monday through Friday 9AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JS

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER